Syllabus
Department of Mathematics and Computer Science
CSC 216: Logic and Switching Theory of the Computer

A. Protocol

Course Name: Logic and Switching Theory of the Computer
Course Number: CSC 216
Credits: 3
Prerequisites: MAT 195 Discrete Mathematical Structures for Computer Science

Upon entering this course the student will be able to:

a) Perform Boolean Algebra manipulations and proofs.
b) Identify sets, subsets, domains, and ranges.
c) Identify and manipulate binary numbers.
d) Create graphs and directed graphs.
e) Discuss combinational and relational structures.
f) Apply a heuristic for problem solving.

Date of Revision: Fall 2004

B. Objectives of the Course

Upon completion of this course the student will be able to:

a) Perform numerical conversions of any base.
b) Identify and convert various non-weighted codes.
c) Identify and convert various weighted codes.
d) Perform binary arithmetic operations.
e) Identify functional components.
f) Form combinational networks and expressions.
g) Construct network diagrams.
h) Identify and apply Boolean connectives.
i) Convert between normal and standard Boolean forms.
j) Apply combinational network analysis and synthesis.
k) Apply the Karnaugh Map minimization technique.
l) Apply the Quine-McCluskey minimization technique.
m) Minimize switching functions with don't care states.
n) Translate networks into all NAND or all NOR logic.
o) Create timing diagrams for sequential networks.
p) Form state transition tables and diagrams.
q) Perform analysis and synthesis of latches and flip-flops.
r) Perform analysis and synthesis of sequential networks.
s) Perform analysis and synthesis of asynchronous networks.
t) Identify encoders, decoders, transcoders, multiplexers, demultiplexers, ROMs and PLAs.
u) Apply network design using encoders, decoders, transcoders, multiplexers, demultiplexers, ROMs and PLAs.

C. Catalog Description

This course provides the student with an in-depth study of the basis of digital computers. Number systems, arithmetic operations, codes, boolean algebra, boolean minimization techniques, state transition tables, and state transition graphs are discussed. Extensive emphasis is placed on the analysis and synthesis of synchronous and asynchronous combinational networks

which form digital computers. Pre requisite: MAT 195 Discrete Mathematical Structures for Computer Science. Three credits.

D. Outline of the Course

a) Numbers ..... 9 hrs
- i) Introduction and Representation of Information]
  - (1) Representation based on distinguishability
  - (2) Representation based on application
  - (3) Representation based on arithmetic
  - (4) Representation based on error control
- ii) Integer Base Conversion
  - (1) Binary to decimal
  - (2) Base x to decimal
  - (3) Decimal to binary
  - (4) Decimal to base x
- iii) Fraction Base Conversion
  - (1) Binary to decimal
  - (2) Base x to decimal
  - (3) Decimal to binary
  - (4) Decimal to base x
- iv) Notations and Conversions
  - (1) Hexadecimal and binary
  - (2) Octal and binary
  - (3) Base y and base x
- v) Codes and Conversions
  - (1) Non-weighted codes
    - (a) ASCII
    - (b) EBCDIC
    - (c) Gray
    - (d) Parity
  - (2) Weighted codes
    - (a) BCD
    - (b) 2421
    - (c) 642-3
    - (d) 2-out-of-5
- vi) Binary Arithmetic operations
  - (1) Addition
  - (2) Subtraction
  - (3) Sign magnitude
  - (4) 1's complement notation
  - (5) 2's complement notation

b) Binary Functions ..... 6 hrs
- i) Functional components
  - (1) Combinational
  - (2) Storage
- ii) Switching functions
  - (1) AND
  - (2) OR
  - (3) INVERTER
  - (4) NAND
  - (5) NOR
  - (6) XOR
  - (7) XNOR
- iii) Combinational networks and expressions
  - (1) Network diagrams

(2) Expressions
iv) Switching Algebra
(1) Boolean connectives
(2) DeMorgan
(3) Normal form
(4) Standard form

c) Combinational Networks ..... 3 hrs
i) Analysis
ii) Synthesis
iii) Translate Networks to all NANDs or all NORs

d) Minimization Techniques ..... 9 hrs
i) Karnaugh maps
ii) Karnaugh maps and don't cares
iii) Quine-McCluskey
iv) Quine-McCluskey and don't cares

e) Combinational Modules ..... 3 hrs
i) Encoders
ii) Decoders
iii) Transcoders
iv) Multiplexers
v) Demultiplexers
vi) ROMs
vii) PLAs

f) Synchronous Sequential Networks ..... 9 hrs
i) Timing diagrams
ii) Latch (Flip Flops)
(1) RS
(2) Master Slave
(3) D
(4) JK
(5) T
iii) Registers
iv) Analysis of sequential networks
(1) State transition tables
(2) State transition diagrams
v) Synthesis of sequential networks
(1) Stuck states
(2) Two level (AND OR) design
(3) Design using combinational modules

g) Asynchronous Sequential Networks ..... 3 hrs
i) Analysis
ii) Synthesis

E. Teaching Methodology

This course will be taught using the lecture/discussion method and cooperative group method during appropriate sections of the course.

F. Assessment Activities

The final grade will be determined as a percentage from the following evaluation methods with varying weights at the discretion of the instructor:

a) Examinations
b) Quizzes
c) Assignments
d) Programs
e) Attendance
f) Performance

G. Accommodations for Students with Disabilities

Students with disabilities:
- Reserve the right to decide when to self-identify.
- Must register with the Office for Students with Disabilities (OSD) to receive services.
- Will provide the appropriate notice from OSD for accommodations which specifically involve the faculty.

Students with disabilities receive services from the Office for Students with Disabilities (OSD). The OSD is located in the Azorsky Building, Room 105. The phone number is (724) 938-5781. Requests for accommodations should be directed to this office and require the student to submit a completed Accommodation Request Form. Approved accommodations will be recorded on the Accommodation Approval Notice and provided to the student.